

1 CLAIMS

WHAT IS CLAIMED IS:

- 5 1. A memory redundancy circuit in a memory module having a designated group of memory cells assigned to represent a logical portion of the memory structure, the memory redundancy circuit, comprising:
 - a. a redundant group of memory cells; and
 - 10 b. a redundancy controller coupled with the designated group and the redundant group, the redundancy controller assigning the redundant group to the logical portion of the memory structure, responsive to a preselected memory group condition.
- 15 2. The memory redundancy circuit of Claim 1, wherein the redundancy controller comprises a redundancy decoder responsive to an encoded signal representative of the preselected memory group condition.
- 20 3. The memory redundancy circuit of Claim 2, wherein the redundancy controller further comprises a plurality of selectable switches, the plurality of selectable switches encoding the preselected memory group condition.
- 25 4. The memory redundancy circuit of Claim 3, wherein the plurality of selectable switches are fuses.
5. The memory redundancy circuit of Claim 4, wherein the preselected memory group condition is a "FAILED" memory group condition, representative of a designated group malfunction.
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6. The memory redundancy circuit of Claim 1, wherein each of the designated group of memory cells and the redundant group of memory cells comprises one of a memory row, a
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- 1 memory column, a preselected portion of a memory module, a
selectable portion of a memory module, a memory module, and
a combination thereof.
- 5 7. The memory redundancy circuit of Claim 1, further
 comprising:
 a. a signal input;
 b. a first memory output coupled with a first memory cell
 group;
10 c. a second memory output coupled with a second memory
 cell group; and
 d. a selector coupled between the signal input, the first
 memory output, and the second memory output, wherein
 the decoder decodes the first memory cell group, and
15 being disposed to select and decode the second memory
 cell group responsive to an group-select signal.
8. The memory redundancy circuit of Claim 7, wherein the
 selector comprises a multiplexer, the multiplexer selecting
20 to decode from one of the first memory cell group and a
 memory second memory cell, the multiplexer being responsive
 to the group-select signal.
9. The memory redundancy circuit of Claim 7, wherein the
25 decoder is a row decoder disposed in a memory module having
 a plurality of adjacent memory rows, and wherein first
 memory row and a second memory row are adjacent memory
 rows in the memory module, and the group-select signal is
 an alternative-row-select signal.
- 30 10. The memory redundancy circuit of Claim 7, wherein the
 decoder is a column decoder disposed in a memory module
 having a plurality of adjacent memory columns, and wherein
 first memory column and a second memory column are adjacent

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1 memory column in the memory module, and the group-select
 signal is an alternative-column-select signal.

11. The memory redundancy circuit of Claim 7, wherein the
5 decoder is a row decoder disposed in a memory module having
 assigned memory rows and a redundant memory row, and
 wherein the first memory row is an assigned memory row, the
 second memory row is the redundant memory row and the
 group-select signal is a redundant-row-select signal.

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12. The memory redundancy circuit of Claim 7, wherein the
 decoder is a column decoder disposed in a memory module
 having assigned memory columns and a redundant memory
 column, and wherein the first memory row is an assigned
15 memory column, the second memory column is the redundant
 memory column and the group-select signal is a redundant-
 column-select signal.

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